REMARKS

In response to the Official Action mailed January 2, 2003, Applicants amend their application and request reconsideration. In this Amendment, no claims are added or canceled so that claims 1-5 remain pending. No new matter has been added.

The Official Action requested correction of the Abstract. The requested corrections were already made in the Preliminary Amendment. If the Preliminary Amendment is not available to the Examiner, a copy will be sent by facsimile upon request. An inadvertent error in the replacement abstract is corrected here. The objections to claims 4 and 5 have been overcome. A proposed drawing amendment accompanies this Amendment.

Claims 1-5 were rejected under 35 U.S.C. 112, second paragraph, as indefinite. That rejection is moot in light of the present Amendment.

Regarding claim 1, the Examiner asserted that the word "some" at line 8 rendered the claim indefinite. Applicants respectfully disagree. The word "some" means, in the English language, fewer than all. There is nothing indefinite about the use of that word in claim 1. Nevertheless, in an attempt to advance the prosecution, the occurrence of "some" has been deleted, and amended claim 1 now simply recites deleting gates from those gates that were inserted.

The Examiner expressed confusion as to the meaning of "collectively" in claims 2 and 3. Applicants intended that word to mean collected in a localized grouping, the conventional meaning of the word. A comparison of Figures 2 and 4 shows that the delay gates of Figure 2 are spaced apart, whereas the delay gates of Figure 4 are clustered together. Again, while there was no error or indefiniteness, to advance the prosecution, claims 2 and 3 have been amended to recite placing a plurality of delay gates proximate one another, as shown in Figure 4.

The Examiner found a lack of relationship between "placing a plurality of delay gates in a region free of lines" and "so that clock lines are not influenced by other lines" in claim 3. Applicants believe the relationship is apparent. Nevertheless, claim 3 has been amended to recite that delay gates are placed into a clock line, thus relating delay gates to clock lines (see page 13, lines 13-14 of the patent application).

The Examiner found a lack of relationship between "stages," "delay gates," and "semiconductor circuit" in claims 4 and 5. Claims 4 and 5 have been amended to recite that the first and last delay gates are not deleted. The term "stage" has been deleted for clarity. Accordingly, claims 1-5 meet all statutory requirements, and the rejections pursuant to 35 USC 112 should be withdrawn.

Claims 1-5 were rejected as unpatentable over Li et al. (U.S. Pat. No. 5,974,245, hereinafter Li). That rejection is respectfully traversed.

Li differs from the present invention in at least two critical ways. First, in Li, clock skew minimization is attempted by inserting only necessary buffers into the circuit before routing takes place (see claim 1, col. 8, lines 22-25, and Figure 4 of Li). By contrast, in the present invention an excess of delay gates are inserted, placed and routed in the circuit, then clock skew is analyzed and delay gates are deleted, as necessary (see Figure 1 of the patent application). Because clock skew analysis is performed after routing in the invention, more accurate adjustment may be made to the circuit in view of timing constraints. Furthermore, the designer does not have to guess or predict where to insert delay gates, or how many, since excess and unnecessary delay gates are simply deleted. Li requires such prediction, and produces a clock skew analysis that is performed before routing.

Li fails to teach or suggest all of the limitations of amended claims 1-5. The Official Action asserts that by moving delay gates after placement, Li must teach or suggest deleting delay gates as recited by amended claim 1. Applicants strongly disagree. Primarily, Li does not suggest the claimed invention because movement of delay gates, and thus any deletion of delay gates, takes place before the circuit is routed, not after as recited in amended claim 1 (see Figure 4 of Li). An analysis of clock skew and timing constraints before routing is not nearly as accurate as such analysis is after routing.

Furthermore, Applicants disagree that a delay gate move equals a delay gate deletion. The total number of delay gates is still the same after a delay gate move, so the invention's advantage of a decrease in the number components is not achieved in a move. Also, Li discloses that only required delay gates are added, so a delay gate cannot be deleted in the sense that it ceases to exist in the circuit. Read in light of the specification, amended claim 1 clearly indicates a reduction in the number of delay gates, not merely the intermediate act of deleting before relocating. The reasoning of the Official Action is erroneous.

Because Figure 4 of Li clearly teaches that any possible deletion of buffers is performed before routing, Li cannot suggest or disclose the method of amended claim 1, which recites that the deletion of delay buffers to meet timing constraints occurs after routing. The effect of this sequence has great bearing on the quality and efficiency of the circuit design.

Second, Li clearly requires a special layout library and a special CAD tool for circuit design. The present invention requires no such special library or tool so that it can be practiced directly, simply, and inexpensively, substantial advantages, not disclosed or suggested by Li.

Accordingly, the *prima facie* obviousness cannot be established by reliance on Li, upon reconsideration, the rejection should be withdrawn.

Respectfully submitted,

Jeffrey A. Wyand, Reg. No. 29,458
LEYDIG, VOIT & MAYER
700 Thirteenth Street, N.W., Suite 300
Washington, DC 20005-3960
(202) 737-6770 (telephone)
(202) 737-6776 (facsimile)

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PATENT
Attorney Docket No. 400966

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

FURUMOTO et al.

Application No. 09/729,088 Art Unit: 2825

Filed: December 5, 2000 Examiner: A. Thompson

For: METHOD OF DESIGNING A SEMICONDUCTOR CIRCUIT WITH REDUCED CLOCK LINE SKEW

AMENDMENTS TO SPECIFICATION, CLAIMS, AND ABSTRACT MADE IN RESPONSE TO OFFICE ACTION DATED JANUARY 2, 2003

Amendments to existing claims:

1. (Thrice Amended) A method of designing a semiconductor circuit having clock trees, the method comprising:

generating a netlist;

inserting a plurality of delay gates into said netlist;

placing said netlist to produce a circuit placement;

generating clock trees for said circuit placement that satisfy a timing constraint;

routing said netlist after generation of said clock trees;

manually adjusting skew between said clock trees after routing by deleting ~~some of said~~ delay gates from the delay gates inserted, based on the timing constraint between said clock trees;

examining the skew between clock trees;

determining whether the timing constraint is satisfied; and

making a minimum change in the placing and routing when said delay gates are inserted.

2. (Twice Amended) The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes ~~collectively~~ placing a plurality of delay gates proximate to one another.

3. (Twice Amended) The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes ~~collectively~~ placing a plurality of delay gates proximate to one another in the same clock line and in a region free of lines, other than clock lines, and free of gates, other than delay gates, so that clock lines are not influenced by other lines.

4. (Thrice Amended) The method of designing a semiconductor circuit according to claim 2, wherein, in manually adjusting skew between clock trees, ~~said delay gates at~~ not deleting the first and last ~~stages among said~~ delay gates ~~inserted are not regarded as targets to be deleted~~ of a clock line.

5. (Twice Amended) The method of designing a semiconductor circuit according to claim 3, wherein, in manually adjusting skew between clock trees, ~~said delay gates at~~ not deleting the first and last ~~stages among said~~ delay gates ~~inserted are not regarded as targets to be deleted~~ of a clock line.

Amendments to the Abstract:

ABSTRACT OF THE DISCLOSURE

In a method of designing a semiconductor circuit having clock trees, a netlist is first generated. Then, delay ~~dates~~ gates are inserted into the netlist. Finally, inserted extra delay gates are deleted so that a timing constraint of the clock trees is satisfied. As a consequence, skew between the clock trees can be easily adjusted.

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PENDING CLAIMS AFTER AMENDMENTS MADE IN RESPONSE TO OFFICE ACTION DATED JANUARY 2, 2003

1. A method of designing a semiconductor circuit having clock trees, the method comprising:

generating a netlist;

inserting a plurality of delay gates into said netlist;

placing said netlist to produce a circuit placement;

generating clock trees for said circuit placement that satisfy a timing constraint;

routing said netlist after generation of said clock trees;

manually adjusting skew between said clock trees after routing by deleting delay gates from the delay gates inserted based, on the timing constraint between said clock trees;

examining the skew between clock trees;

determining whether the timing constraint is satisfied; and

making a minimum change in the placing and routing when said delay gates are inserted.

2. The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes placing a plurality of delay gates proximate to one another.

3. The method of designing a semiconductor circuit according to claim 1, wherein placing said netlist includes placing a plurality of delay gates proximate to one another in the same clock line and in a region free of lines, other than clock lines, and free of gates, other than delay gates, so that clock lines are not influenced by other lines.

4. The method of designing a semiconductor circuit according to claim 2, wherein, in manually adjusting skew between clock trees, not deleting the first and last delay gates of a clock line.

5. The method of designing a semiconductor circuit according to claim 3, wherein, in manually adjusting skew between clock trees, not deleting the first and last delay gates of a clock line.